

Remarks

Claims 23-48 were rejected as or unpatentable over KUDO et al. 6,853,037 in view of O 7,088,964 and the admitted prior art (APA). Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 23 provides, among other features, that the MOS varactor film (the second insulating film) is thinner than the thinnest of the MOS transistor films (the first insulating films), where the MOS transistor films have a plurality of different thicknesses. Thus, the second insulating film is thinner than all the first insulating films. The references do not disclose this.

KUDO et al. disclose a semiconductor device with a plurality of MOS transistors having different gate insulating film thicknesses. The film thickness of the n-channel high-voltage transistor is greater than the film thickness of the p-channel high voltage transistor, which is greater than the film thickness of the low-voltage transistor (Abstract). KUDO et al. do not disclose a film thickness of a varactor.

O discloses that CMOS varactors are generally formed using design rules for logic devices and that logic devices are generally significantly smaller than I/O devices and use a thinner gate oxide (column 11, lines 17-21). That is, the film thickness of the I/O transistor is thicker than that of the film

thickness of a logic transistor, and the film thickness of the varactor is equal to that of the logic transistor.

The APA acknowledges that logic devices and I/O devices are generally formed on the same chip.

Thus, KUDO et al. disclose only the film thicknesses of the transistors, and O discloses that the logic transistor has a film thickness equal to that of the varactor. Combining the references does not suggest to the artisan that the film thicknesses of all the MOS transistors are each to be greater than that of the varactor.

That is, the combination of these three references disclose that in a chip with logic devices and I/O devices, the thinnest gate insulating films among the MOS transistors is to be found in the logic devices. The combination merely discloses that the gate insulating film of the varactors element is the same thickness as that of a gate insulating film of the thinnest MOS transistor on the chip. There is nothing in the combination that discloses that the thickness of the second gate insulating film in the varactor element is thinner than the thinnest gate insulating film among the first gate insulating films of the MOS transistors with different thicknesses.

The Official Action notes that "[a]ny of the MOS structures can be labeled as a transistor or varactor." However, the varactor is specifically defined in the fourth and last

paragraphs of claim 23. As is known, a MOS transistor does not have the varactor structure defined in the claim.

The Official Action also notes that "[m]ere labeling will not distinguish these claims over the applied art." The claims do define the varactor structure in a manner that is distinguishable from the MOS transistors and thus the claims go beyond "mere labeling." Indeed, the application is written for one of skill in the art for whom the words in the claims have meaning; the words are not like soft wax that can take any shape.

Claim 36 provides that the MOS transistor films all have a same thickness. Thus, the second insulating film is thinner than all the first insulating films. The references do not disclose this. As explained above, the I/O transistor film thickness is greater than that of the logic film thickness, where the logic film thickness is the same as, not less than, the varactor film thickness.

Accordingly, the claims avoid the rejection under §103.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment

to Deposit Account No. 25-0120 for any additional fees required
under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON

/Thomas W. Perkins/
Thomas W. Perkins, Reg. No. 33,027
209 Madison Street, Suite 500
Alexandria, VA 22314
Telephone (703) 521-2297
Telefax (703) 685-0573
(703) 979-4709

TWP/dp